CLAIMS

What is claimed is:

1. A method comprising:

detecting an error of a transmission of an interconnect;

retrying the transmission in response to the detected error;

detecting a hard failure if the retrying is unsuccessful; and

reducing a transmission width of the interconnect in response to the detected hard failure.

2. The method according to claim 1, wherein the reducing of the transmission width comprises selecting a working portion of the interconnect in response to the hard failure.

3. The method according to claim 1, wherein the detecting of the hard failure provides an indication of failed portions of the interconnect, and the reducing selects a working portion of the interconnect based on the indication of failed portions.

4. The method according to claim 1, wherein the detecting of the transmission error is performed using a cyclic redundancy check.

5. The method according to claim 1, further comprising replacing the interconnect with a replacement interconnect after the transmission width is reduced.

6. The method according to claim 1, further comprising retrying the transmission after the transmission width is reduced.

7. The method according to claim 1, wherein the interconnect is a bus.

8. An apparatus comprising:

a transmission error detector to detect an error of a transmission of an interconnect;

a transmitting agent to retry the transmission in response to the detected error;

a hard failure detector to detect a hard failure of the interconnect if the retry is unsuccessful; and

a transmission width reducer to reduce a transmission width of the interconnect in response to the hard failure detector.

9. The apparatus according to claim 8, wherein the transmission width detector is to select a working portion of the interconnect in response to the hard failure detector.

10. The apparatus according to claim 8, wherein the hard failure detector is to indicate failed portions of the interconnect, and the transmission width detector is to select a working portion of the interconnect based on the indicated failed portions.

11. The apparatus according to claim 8, wherein the transmission error detector is to perform a cyclic redundancy check.

12. The apparatus according to claim 8, the transmitting agent to retry the transmission after the transmission width is reduced.

13. The apparatus according to claim 8, wherein the interconnect is a bus.

14. The apparatus according to claim 8, wherein the interconnect is an input/output bus.

15. An interconnect comprising:

a transmission width to transmit information;

a transmission error detector to detect a transmission error of the interconnect;

a transmitting agent to retry a transmission in response to the detected error;

a hard failure detector to detect a hard failure of the interconnect if the retry is unsuccessful; and

a transmission width reducer to reduce a transmission width of the interconnect in response to the hard failure detector.

16. The interconnect according to claim 15, wherein the transmission width detector is to select a working portion of the interconnect in response to the hard failure detector.

17. The interconnect according to claim 15, wherein the hard failure detector is to indicate failed portions of the interconnect, and the transmission width detector is to select a working portion of the interconnect based on the indicated failed portions.

18. The interconnect according to claim 15, wherein the transmission error detector is to perform a cyclic redundancy check.

19. The interconnect according to claim 15, the transmitting agent to retry the transmission after the transmission width is reduced.

20. The interconnect according to claim 15, wherein the interconnect is a bus.

21. The interconnect according to claim 15, wherein the interconnect is an input/output bus.

22. A system comprising:

a first component;

a second component; and

an interconnect comprising:

a transmission width to transmit information between the first component and the second component;

a transmission error detector to detect a transmission error of the interconnect;

a transmitting agent to retry a transmission in response to the detected error;

a hard failure detector to detect a hard failure of the interconnect if the retry is unsuccessful; and

a transmission width reducer to reduce a transmission width of the interconnect in response to the hard failure detector.

23. The system according to claim 22, wherein the transmission width detector is to select a working portion of the interconnect in response to the hard failure detector.

24. The system according to claim 22, wherein the hard failure detector is to indicate failed portions of the interconnect, and the transmission width detector is to select a working portion of the interconnect based on the indicated failed portions.

25. The system according to claim 22, wherein the transmission error detector is to perform a cyclic redundancy check.

26. The system according to claim 22, the transmitting agent to retry the transmission after the transmission width is reduced.

27. The system according to claim 22, wherein the interconnect is a bus.

28. The system according to claim 22, wherein the interconnect is an input/output bus.

29. The system according to claim 22, wherein the first component is a processor, a memory, a chip set, a memory bridge, an I/O device or an I/O hub and the second component is a processor, a memory, a chip set, a memory bridge, an I/O device or an I/O hub.